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| APPLICATION NO. | FILING DATE | FIRST NAMED INVENTOR | ATTORNEY DOCKET NO. | CONFIRMATION NO. |
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| 10/787,269 | 02/25/2004 | Chien-Ping Huang | 58102-DIV (71987) | 5161 |

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| EXAMINER | |
|---|---|
| CAO, PHAT X | |

| ART UNIT | PAPER NUMBER |
|---|---|
| 2814 | |

DATE MAILED: 09/09/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

| Office Action Summary | Application No. | Applicant(s) | |
|---|---|---|---|
| | 10/787,269 | HUANG, CHIEN-PING | |
| | Examiner | Art Unit | |
| | Phat X. Cao | 2814 | |

*-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --*

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

1)☒ Responsive to communication(s) filed on *25 February 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

4)☒ Claim(s) *16-45* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *16-45* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

**Application Papers**

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☒ Certified copies of the priority documents have been received in Application No. 10/211,430.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *2/25/04*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

## DETAILED ACTION

1. The cancellation of claims 1-15 in Paper filed on 2/25/04 is acknowledged.

### *Claim Rejections - 35 USC § 103*

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. Claims 16-24, 26-33, 35-41, and 43-45 are rejected under 35 U.S.C. 103(a) as being unpatentable over Huang et al (US. 2002/0113308) in view of Applicant's admitted prior art.

Regarding claims 16, 29, and 38, Huang (Figs. 5 and 9) discloses a heat dissipating structure for a semiconductor package having a substrate 30, at least a chip 51 mounted on the substrate 30 and electrically connected to the substrate 30 via a plurality of conductive wire elements 22, the heat dissipating structure 331 comprising: a flat portion; and a plurality of support portions 330 formed at edged of the flat portion 331 for supporting the flat portion in position above the chip 51, wherein the support portions 330 are mounted at a predetermined area on the substrate 30 and free of interference with an arrangement of the chip 51, and the conductive wire elements 22, and the support portions 330 are arranged to form a space between two adjacent support portions (see Fig. 9), the space being sufficiently dimensioned to accommodate the conductive wire elements 22 so as to allow the conductive wire elements 22 to pass

through the space to reach an area on the substrate 30 outside coverage of the heat dissipating structure (also see Fig. 9).

Huang does not disclose a passive component mounted on the substrate 30.

However, Applicant's admitted prior art (Fig. 5) teaches a semiconductor package having a chip 31, and passive components disposed on the substrate 30 (not shown, see Applicant's specification, page 2, lines 11-13). Accordingly, it would have been obvious to form the passive components on the substrate of Huang in order to provide a desired semiconductor package, which has a required layout for the integrated circuit.

Regarding claims 17, 19 and 21, Huang (Fig. 5) further discloses that: the conductive elements are bonding wires 22; a plurality of bond fingers 202 (not labeled in Fig. 5, see Fig. 3) are formed on the substrate 30 for allowing the bonding wires 22 to be bonded to the bond fingers 202, wherein part of the bond fingers 202 are situated on the substrate 30 at an area outside the coverage of the heat dissipating structure, allowing the corresponding bonding wires 22 to pass through the space embraced by adjacent support portions 330 and the flat portion 331 and to reach the outside-coverage bond fingers (see Fig. 9); and the chip 51 and the conductive wire elements 22 are encapsulated by an encapsulant 35 formed on the substrate 30.

Regarding claims 18, 22, 24, 30, 32, 33, 40 and 41, Huang (Fig. 5) further discloses that: the flat portion 331 is elevated above the chip 51 by the support portions 330 and forms a predetermined height difference with respect to the substrate 30, allowing the height difference to be larger than a height of wire loops of the bonding

wires 22; the flat portion 331 has a top surface exposed to outside of the encapsulant 35, and a bottom surface opposed to the top surface, the bottom surface being formed with the support portions 330; and a peripherally-situated recess 331d is formed on the top surface of the flat portion 331.

Regarding claims 20, 23, 31 and 39, Huang further discloses that the support portions 330 are situated at edge corners of the flat portion (see Fig. 2), and a protrusion 531e is formed on the bottom surface of the flat portion and extends toward the chip 51 (see Fig. 6).

Regarding claims 26-28, 35-37 and 43-45, Huang (Fig. 5) also discloses that each of the support portions 330 is formed with a contact portion at a position in contact with the substrate 30, the contact portion is a semicircular shape and extends laterally with respect to the substrate 30.

3. Claims 16-45 are rejected under 35 U.S.C. 103(a) as being unpatentable over Chiang et al (US. 5,736,785) in view of Applicant's admitted prior art.

Regarding claims 16, 20, 29 and 38, Chiang (Figs. 4A-4E) discloses a heat dissipating structure for a semiconductor package having a substrate 104, a chip 102 mounted on the substrate 104 and electrically connected to the substrate 104 via a plurality of conductive wire elements 108, the heat dissipating structure 116 comprising: a flat portion 116; and a plurality of support portions 116f/116c (see Fig. 4C and column 4, lines 38-40 and lines 51-55) formed at edge corners of the flat portion for supporting the flat portion in position above the chip, wherein the support portions 116c are mounted at a predetermined area on the substrate 104 and free of interference with an

arrangement of the chip 102 and the conductive wire elements 108 (see Fig. 4C and column 4, lines 51-55), and the support portions 116c are arranged to form a space between two adjacent support portions 116c, the space being sufficiently dimensioned to accommodate the conductive wire elements 108 so as to allow the conductive wire elements 108 to pass through the space to reach an area on the substrate 104 outside coverage of the heat dissipating structure 116 (see Fig. 4C).

Chiang does not disclose a passive component mounted on the substrate 104.

However, Applicant's admitted prior art (Fig. 5) teaches a semiconductor package having a chip 31, and passive components disposed on the substrate 30 (not shown, see Applicant's specification, page 2, lines 11-13). Accordingly, it would have been obvious to form passive components on the substrate of Chiang in order to provide a desired semiconductor package which has a required layout for the integrated circuit.

Regarding claims 17, 19 and 21, Chiang further discloses that: the conductive elements are bonding wires 108; a plurality of bond fingers (i.e., conductive traces) are formed on the substrate 30 for allowing the bonding wires 108 to be bonded to the bond fingers (column 4, lines 14-16), wherein part of the bond fingers are situated on the substrate 30 at an area outside the coverage of the heat dissipating structure 116, allowing the corresponding bonding wires 108 to pass through the space embraced by adjacent support portions 116c/116f and the flat portion and to reach the outside-coverage bond fingers (i.e., conductive traces) (see Fig. 4C); and the chip 102 and the

conductive wire elements 108 are encapsulated by an encapsulant 112 formed on the substrate.

Regarding claims 18, 22, 24, 30, 32, 33, 40 and 41, Chiang further discloses that: the flat portion 116 is elevated above the chip 102 by the support portions 116c and forms a predetermined height difference with respect to the substrate 104, allowing the height difference to be larger than a height of wire loops of the bonding wires 108 (see Fig. 4A); the flat portion 116 has a top surface exposed to outside of the encapsulant 112, and a bottom surface opposite to the top surface, the bottom surface being formed with the support portions 116c; and a peripherally situated recess formed between the adjacent raised portions 116d is formed on the top surface of the flat portion (see Fig. 4E).

Regarding claims 23, 31, and 39, Chiang further discloses that a protrusion 116a is formed on the bottom surface of the flat portion and extends toward the chip 102 (see Figs. 4B and 4E).

Regarding claims 26-28, 35-37 and 43-45, Chiang (Fig. 4A) also discloses that each of the support portions 116c is formed with a contact portion at a position in contact with the substrate 104, the contact portion is a semicircular shape and extends laterally with respect to the substrate 104.

Regarding claims 25, 34, and 42, Chiang (Fig. 4C) also discloses that each of the support portion 116f/116c is formed with a hole 116b for allowing an encapsulating resin used for forming the encapsulant to pass through the hole 116b (column 4, lines 64-67).

***Double Patenting***

4. The nonstatutory double patenting rejection is based on a judicially created doctrine grounded in public policy (a policy reflected in the statute) so as to prevent the unjustified or improper timewise extension of the "right to exclude" granted by a patent and to prevent possible harassment by multiple assignees. See *In re Goodman*, 11 F.3d 1046, 29 USPQ2d 2010 (Fed. Cir. 1993); *In re Longi*, 759 F.2d 887, 225 USPQ 645 (Fed. Cir. 1985); *In re Van Ornum*, 686 F.2d 937, 214 USPQ 761 (CCPA 1982); *In re Vogel*, 422 F.2d 438, 164 USPQ 619 (CCPA 1970); and *In re Thorington,* 418 F.2d 528, 163 USPQ 644 (CCPA 1969).

A timely filed terminal disclaimer in compliance with 37 CFR 1.321(c) may be used to overcome an actual or provisional rejection based on a nonstatutory double patenting ground provided the conflicting application or patent is shown to be commonly owned with this application. See 37 CFR 1.130(b).

Effective January 1, 1994, a registered attorney or agent of record may sign a terminal disclaimer. A terminal disclaimer signed by the assignee must fully comply with 37 CFR 3.73(b).

5. Claims 16-45 are rejected under the judicially created doctrine of obviousness-type double patenting as being unpatentable over claims 1-15 of U.S. Patent No. 6,720,649. Although the conflicting claims are not identical, they are not patentably distinct from each other because both U.S. Patent and instant application disclose a heat dissipating structure for a semiconductor package, the heat dissipating structure comprising: a flat portion; and a plurality of support portions formed at edges of the flat portion for supporting the flat portion in position above the chip, the support portions are arranged to form a space between adjacent support portions, the space being sufficiently dimensioned to accommodate the conductive wires and the passive components so as to allow the conductive wires to pass through the space to reach an area on the substrate outside coverage of the heat dissipating structure. Moreover, the claims in the instant application are either broader versions of the claims in U.S. Patent 6,720,649 or are obvious variations thereof.

6. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Phat X. Cao whose telephone number is 571-272-1703. The examiner can normally be reached on M-F.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Wael Fahmy can be reached on 571-272-1705. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

PC
September 2, 2005

PHAT X. CAO
PRIMARY EXAMINER